IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

D. Chidambarrao, et al.

Docket No.: FIS920030185US

Serial No.: 10/605,167

Group Art Unit: 2282

Filed: September 12, 2003

Examiner: Pamela Perkins

For: MOSFET PERFORMANCE IMPROVEMENT USING DEFORMATION IN SOI STRUCTURE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

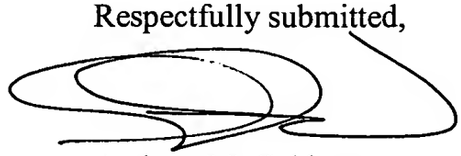
Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. A copy of the cited documents is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's deposit account no. 23-1951 (McGuireWoods LLP).

Respectfully submitted,



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Supplemental Form PTO-1449 (Modified)	Attorney Docket No.: FIS920030185US1	Serial No.: 10/605,167
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Applicant: D. Chidambarrao, et al.	
(Use several sheets if necessary) Page 1 of 1	Filing Date: September 12, 2003	Group: 2822

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

			Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si *n*-MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
			Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
			Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
			F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
			Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
			A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
			K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.